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PLANAR METAL ELECTROPROCESSING

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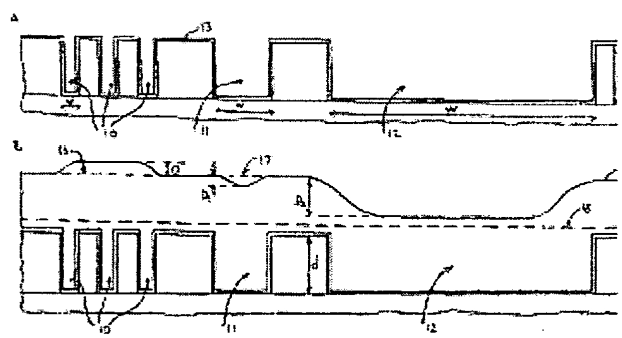
The present invention relates to a method for forming a planar conductive surface on a wafer. In one aspect, the present invention uses a no-contact process with electrochemical deposition, followed by a contact process with electrochemical mechanical deposition. In another aspect the no-contact process with electrochemical deposition uses a solution tailored to this no- contact process, and the contact process with electrochemical mechanical deposition uses a different solution tailored to this contact process.



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PLANAR METAL ELECTROPROCESSING 1. FIELD OF THE INVENTION [0001] The present invention relates to manufacture of semiconductor integrated circuits and, more particularly to a method for planar deposition and polishing of conductive layers.

2. DESCRIPTION OF THE RELATED ART [0002] Conventional semiconductor devices generally include a semiconductor substrate, such as a silicon substrate, and a plurality of sequentially formed dielectric interlayers such as silicon dioxide and conductive paths or interconnects made of conductive materials.

Copper and copper-alloys have recently received considerable attention as interconnect materials becau of their superior electro-migration and low resistivity characteristics. The interconnects are usually form by filling copper in features or cavities etched into the dielectric layers by a metallization process. The preferred method of copper metallization is electroplating. In an integrated circuit, multiple levels of interconnect networks laterally extend with respect to the substrate surface. Interconnects formed in sequential layers can be electrically connected using vias or contacts.

[0003] In a typical process, first an insulating layer is formed on the semiconductor substrate. Patterning and etching processes are performed to form features or cavities such as trenches and vias in the insulati layer. Then, a barrier/glue layer and a seed layer are deposited over the patterned surface and a conductc such as copper is electroplated to fill all the features.

However, the plating process, in addition to filling the features with copper, also deposits excess copper over the top surface of the substrate. This excess copper is called an"overburden"and needs to be remov during a subsequent process step. In standard plating processes this overburden copper has a large topography since the Electrochemical Deposition (ECD) process coats large features on the wafer in a conforma manner. For example, a wafer with 0.5 micron deep features may be coated with 0.8 micron thick copper by the standard ECD process, to assure complete, defect-free filling of all the features, including those that are wider than about 5 microns. The resulting copper surface then may have a topography that has a step of about 0.5 microns over the large features. Conventionally, after the copper plating, CMP process is employed to first globally planarize this topographic surface and then to reduce the thickness of the overburden copper layer down to the level of the surface of the barrier layer, which also later removed leaving conductors only in the cavities. CMP is a costly and time consuming process High pressures used in the CMP processes also damage low-k dielectrics, which are mechanically weak than the silicon oxide. Therefore, minimizing CMP step in an integration process is a goal forall IC manufacturers. The topography on the wafers also causes problems for the CMP process. Specifically, tl large steps such as the0. 5 micron step of the above example over the large features such as 100 micron wide trenches or bond-pads, cause dishing defects after CMP. Therefore, both in terms of cost and enabling features, it is very attractive to have processes that have the ability to yield thinner copper deposits with reduced surface topography on wafers.

[0004] During the copper electrodeposition process, specially formulated plating solutions or electrolyte are used. These electrolytes typically contain water, acid (such as sulfuric acid), ionic species of copper, chloride ions and certain additives which affect the properties and the plating behavior of the deposited material. Typical electroplating baths contain at least two of the three types of commercially available additives such as accelerators, suppressors and levelers. It should be noted that these additives are sometimes called different names. For example, the accelerator may be referred to as a brightener and tl suppressor as a carrier in the literature. Functions of these additives in the electrolyte and the role of the chlorideion are widely known in the field (see for example, Z. W. Sun and G. Dixit, "Optimized bath control for void-free copper deposition", Solid State Technology, November 2001, page. 97), although t details of the mechanisms involved may not be fully understood or agreed upon.

[0005] Electrodeposition process needs to fill all the features, small and large, on the substrate. Figure1 schematically shows the cross sectional view of an exemplary wafer surface with high-aspect ratio vias a medium aspect-ratio trench11, and a small aspect-ratio pad 12, coated with abarrier/seed layer 13, whi

is shown as one layer to simplify the drawing. As is well known in the field, aspect ratio is the ratio of tl depth, d, of the features to their smaller lateral dimension or width, w. In our example the depth, d may range from 0. 1 microns to 2.0 microns, although deeper features may also be used for certain applicatio such as packaging applications. The width of the vias 10 may be sub-micron in size and their aspect rati (d/w) may be in the range of 1-10. The trench 11 may have an aspect ratio of 0.1-1 and the pad 12 may have an aspect ratio of less than 0.1. For a feature depth of for example 0.5 microns, the vias may be 0.1 micron wide, the trench 11 may be 2 micron wide and the pad may be 20 microns wide.

[0006] Figure1B shows the substrate of Figure 1A after copper deposition carried out by prior art metho The solid line 15 indicates the typical topography of the copper film resulting from a typical ECD proce employing an additive package containing two additives, accelerator and suppressor species. It is well known that these additives help bottom-up filling of the high aspect-ratio vias 10 with copper. The mechanism of bottom-up fill, however, becomes less and less effective as the aspect ratio of the features become smaller and smaller, and the deposition becomes more and more conforma. The result is shown Figure 1 B as a small step
Dl over the medium size feature or trench 11 and a large step D2 over the large feature or pad 12. It shoı be noted that magnitude of these steps over the various size features is at most as large as the feature de| d. The over-fill,O, shown over the dense array of vias 10 is typically observed in copper films deposited the electrolytes containing two-component additive package of this example. As can be seen in Figure1] the surface topography of the copper film is large and this presents challenges in the CMP step as described earlier.

[0007] Several developments have been provided by prior art methods to improve the copper topograph depicted by the solid line 15 in Figure 1B. To reduce or eliminate the over-fillO, a third additive, levelei added into the electrolyte formulation. By controlling the concentration of the additive carefully, the profile of copper over the dense array of vias 10 could be made flat, which is shown as the dotted line 1ı Figure 1B. U. S. Patent 6,346, 479 B1 describes a method where copper is deposited in anon-conformal electroplating process to fill a portion of the features. A second electroplating process is then performed toconformally deposit copper in the remaining unfilled portion of the openings or features. Such an approach may yield a flat profile over dense array of small features such as vias 10 of our example, as w as possibly over the medium size features such as trench 11 of our example as depicted by dotted lines 1 and 17, respectively. However, as disclosed in U. S. Patent 6,346, 479Bl the second electroplating processconformally deposits copper over the substrate, and therefore can not eliminate the large step D2 over the large features such as the pad 12 shown in our example of
Figure1B. U. S. Patent 6,350, 364 Bl describes a method of electroplating copper in trenches where a fiı copper deposition step has a first ratio of brightener-to-leveler concentration and a second copper deposition step has a second ratio of brightener-to-leveler concentration that is less than the first ratio of brightener-to-leveler concentration. This way it is reported that the stepDl of Figure 1B can be reduced. is well known in the field copper electroplating additives are not operative in the very large features witl very small aspect-ratios such as the pad 12 of
Figure 1 B. Therefore, the step D2 is not expected to be much reduced or eliminated by such approache: D2 only gets reduced and eliminated if a very thick copper layer with thickness value close to half the width of the largest feature on the wafer is plated (see e. g. U. S. Patent 5,256, 565, October 26,1993). However, this is not practical considering the fact that many interconnect designs involve feature sizes v above 10 microns.

[0008] As the above review demonstrates, some of the prior-art techniques aiming to obtain relatively fl copper topography on patterned wafer surfaces may be applicable for the class of wafers with large or medium aspect-ratio features. However, manyIC interconnect designs contain features with a wide varie of aspect ratios on a given wafer surface. Especially in multi-level interconnect structures the width of tl high-current-carrying lines increase while their aspect-ratios decrease at the higher wiring levels.

Therefore, an approach that has the capability of reducing or eliminating surface topography of copper over features with a large range of aspect ratios is needed.

[0009] A technique that can reduce or totally eliminate copper surface topography for all feature sizes is the Electrochemical Mechanical Processing (ECMPR). This technique has the ability to eliminate steps 1, D2 and overfill O shown in the example of Figure 1B, and provide thin layers of planar conductive material on the workpiece surface, or even provide a workpiece surface with no or little excess conducti material. This way, CMP process can be minimized oreven eliminated. The term"Electrochemical Mechanical Processing (ECMPR) "is used to include both Electrochemical Mechanical Deposition (ECMD) processes as well as
Electrochemical Mechanical Etching (ECME), which is also called Electrochemical Mechanical Polishing <RTI (EC W). It is understood that the second cavity 406 may be any cavity that is partially filled and that can be used to determine if the D > W condition exists. The no-contact plating may be continued as long as D > W condition exists in any of the cavities. Preferably, contact plating may not b initiated as long as the D > W condition exists. As will be described below, if the contact plating is initiated with D > W condition existing, defects may form.

[00043] Accordingly, as shown in Figures 6A and 7, depending on the process parameters used, no cont plating may result in a second layer 420 having two types of surface profile, namely flat profile (Figure 6A) and overfill profile (Figure 7) respectively. In the preferred flat profile, as shown in Figure 6A, as tl no-contact plating process is continued and the second layer 420 is coated on the first layer 418, the asp ratio of the second cavity 406 is smaller such that the width W of the cavity becomes larger than the dep D. That is, W > D condition exists. This condition may also be expressed in terms of the thickness of th selected regions of the deposited layer and the corresponding growth rate for that selected thickness valı

As shown in Figure 6B, if rb is the growth rate from the bottom wall of the second cavity 406 andrw is t growth rate from the top of the side walls of the second cavity 406, the above given condition W > D ca also be expressed approximately asWo-2 rw t > (Do-rb t), where Wo and Do are the initial width and th depth of the cavity before the deposition, and t is the deposition time.

It should be noted that the barrier and seed layers are not shown in any of the figures for the purpose of clarification.

[00044] Referring to the case of overfill profile (Figure 7), as the no-contact plating fills the first cavity 404 an overfill feature 421 such as a bump may form above the first cavity 404.

During the copper plating process, such bumps are possible and formed due to the overfilling of the cavities. Although mechanism is not fully understood, it is believed that such bumps form due to preferential or accelerated adsorption of growth accelerating additive species in the small cavities. In su morphologies, due to the existence of the bump 421, in the subsequent contact plating stage, as opposed the case of the flat profile, a thick deposition layer is required to fill the cavities 406,408 and to cover th bump 421. This is time consuming and reduces system efficiency. Therefore, the flat profile is the preferred surface profile in this embodiment.

However, if the bumps are formed, the second step of the process eliminates them by planarizing the surface.

[00045] Referring back to Figure 6A, flatness of the second layer 420 may be obtained using various techniques such as using flatness enhancing agents in the electrolyte solution or using a pulse power supply to energize the anode and the cathode. Flatness enhancing agents may be exemplified as levelers Levelers are well known chemicals in the electroplating technology and used to effectively suppress the

growth of bumps on the depositing layers. A pulse power supply or a variable voltage power supply can also minimize or eliminate the over fill bump. A technique called reverse pulse plating process may be used to obtain flat surface profiles over small features. In this approach, the voltage pulses make the workpiece surface periodically cathodic to deposit copper on it and anodic for a shorter time to etchback portion of the deposited material so that flatness of the layer can be achieved. The pulse power supply c: also be used during the second step or the contact plating and third step or the electroetching step of the process of the present invention. Referring back to Figures 6A and 6B, once theWo-2 r, t > (Do-rb t) condition is satisfied for all the remaining features (i. e. , the mid-size and the large features), the proces continued with the"contact"plating stage of the process, or a second stage of the process, to completely 1 the cavities. At the"contact"plating stage of the process, the front surface110 is contacted to the top surf: of the mask plate 102, while the deposition process continues. If the contact plating is initiated without satisfying the W > D condition, defects may form.

[00046] Figures 8A and 8B exemplifies formation of such defects. As shown in Figure 8A, when the contact plating is initiated the mask plate 102 sweeps or mechanically influences the top portion 418A o the layer 418 but not an inner portion 418B and a mouth portion418C covering the second cavity 406 si walls and the bottom wall. This in turn reduces the growth rate at the top portion 418A in comparison to both the inner portion 418B and the mouth portion418C. Further the mechanical influence increases late growth rate of the copper at the mouth portion 418C in comparison to the inner portion41 SB since it creates an additive differential between the inner portion 418B. This situation can be seen in Figure 8B where as consecutive layers 419A, 419B, 419C are coated with contact plating, the layers 419A-419C grow faster at locations covering the mouth portion418C than the inner portion 418B. Portions of the layers 419A-419C covering the top portion 418A grow slowly due to the mechanical influence created t the contacting mask plate. Such non conforma growth pattern eventually forms a defect 423, often a hol entrapping electrolyte solution which is an unwanted situation in electroplating.

[00047] As shown in Figure 9, the mechanical influence created by the contacting mask plate 102 furthe planarizes the growing deposition layer, and if the overfill profile is used, the mechanical influence removes the bump 421 as well (see Figure 7). This results in a third deposition layer 424, which is a substantially planarized layer, on the workpiece106. The contact step of the process may proceed in sucl manner that theworkpiece 106 may makecontact with the mask plate 102 intermediately (i. e. , in a discontinuous fashion). This still results in planarized layer and smoothes the top layer. Further, such contact and no-contact action may be repeated multiple times.

[00048] In the following stage of the process, by reversing the polarization of theelectrodes (i. e. , by applying negative potential to anode electrode and by applying positive potential to the workpiece), the layer 424 can be electroetched down to a predetermined thickness over the interlayer regions. In this thi step, electroetching process may be performed using the same electrolyte solution used during the electrodeposition stage and using the same system above. As in the case of electrodeposition, the electroetching may be also carried out by"nocontact"electroetching and"contact"electroetching process steps. Accordingly, as illustrated in
Figure 10, with the no-contact electroetching process, thickness'd'of the layer 424 can be reduced down thickness A in a planar manner. As illustrated in Figure11, with the application of the contact electroetching process, contacting mask plate 102 reduces the thickness of the layer 424 in a planar fashion, down to thickness B.

[00049] Contact and no-contact electroetching can be used sequentially and multiple times using the sar or different process parameters such as by employing different current levels, different wafer pressure levels and different rotational and lateral velocities. If contact and no-contact electroetching processes a performed in a multiple fashion, the process may be terminated with contact electroetching process. As mentioned above, the contact step smoothes the layer. The thickness B may be less than the depth Do of

the cavities 404,406 and 408, and preferably less than half of the depth (Do/2) of the cavities. The third step of the process may be performed in the same electrolyte or solution that is used for the deposition process. Further, this step may be performed in the same process module that the deposition is carried o and subsequent to the deposition process.

[00050] The method of the above embodiment can fill cavities of any shape and form.

One example, a dual damascene structure 500, is shown. in Figure 12. The dual damascene structure 50 has a via 502 and a trench 504 formed in an insulator 506. The via 502 may be a narrow via, and the tre 504 may be a mid size or a larger trench. If the above process is used, in first step of the process or no contact step, the depositing material fills the via 502 andconformally coats the trench 504 with a first la 508. In a second step, or contact step, of the process, the depositing material fills the trench completely with a second layer510 and the mechanical influence created by the contacting mask plate 102planarize the growing second layer 510. In the third step, a layer 512 that is formed by sequentially depositing lay 508 and 510 is electroetched down to a predetermined thickness'C"as shown in Figure 12.

[00051] Different Solution Process Sequence [00052] The embodiment that uses different solutions for no-contact process with electrochemical deposition and the contact process with electrochemical mechanical deposition will now be described.

[000531 Figure 13A shows the front surface 110 of the wafer 106 as it is electroplated using a first electroplating solution 120. The surface 110 may include small features 122, a mid size feature 124 and large feature126. The small size features may have a width less than a micron while the mid size feature may have 1 to 5 micron width range. Large features may have a width larger than 10 microns. The featu 122,124, 126 are formed in an insulating layer 128 that is formed on the semiconductor wafer 106. A barrier layer 130 such as Ta, TaN or their composite Ta/TaN coats the inside of the features and the top surface 132 of the insulating layer128. The top surface 132 is also called the"field region". A seed layer (not shown) such as a thin copper layer is coated on the barrier layer. During the process, the wafer 106 placed away from the WSID (no-touch plating) and the first electroplating solution is flowed through th WSID to wet the front surface 110 of the wafer106 while the wafer is rotated and movedlaterally. Once electrical potential applied between the wafer and the electrode, i. e. , anode, (shown in Figure 2), a first copper layer 134a is formed. The first copper layer 134a fills the small and mid size features in bottom- fashion butconformally coats the large feature because of its large width.

[00054] In the first stage of the process, the WSID acts as a shaping plate. It is important that the chann of the WSID not only allows the process solution to flow to the surface of the wafer, but also shapes the plating current density and thus the resulting thickness profile of the deposited copper layer. The distribution, shape and size of the openings may introduce regions of low, intermediate, and high deposition rates above the WSID. By movingthe wafer over these regions during the process a desired thickness profile, e. g. , a uniform thickness profile, of the depositing layer is obtained. An exemplary process of thickness profile control is disclosed inU. S. Patent Application No. 09/760,757 filed on Janu 17,2001 entitled"Method and Apparatus for Electrodeposition of Uniform Film on Substrate, "which is commonly owned by the assignee of the present invention. If desired, this plating step can be carried ou without the WSID if other means are provided to yield a uniform deposit.

[00055] In this embodiment, the first electroplating solution 120 may comprise at least two additives to enhance bottom up filling of the small features without any voids, seams and other defects. For example high-acid plating electrolyte containing 0.8-2mol/1 of Cubath (g ViaFormTM Accelerator available fromEnthone-OMIC, West Haven, CT and 6-12mol/1 ofCubath (1 ViaForm Suppressor marketed by the same company may be used in the basic plating bath chemistry which contains sulfuric acid, copper sulfate, water and chloride ions. Low acid versions of the plating chemistry may require quite different

concentrations of accelerators and suppressors (such as an accelerator concentration of about 4-8 ml/l, a suppressor concentration of 2-4ml/1 for the case of Enthone low acid chemistry). During the process, th accelerators allow bottom up growth of copper in the small features that are filled quickly. The suppress molecules which are adsorbed at the top of the openings of the small features slow down the copper gro therein, thus avoiding both premature closing of these passages and formation of voids. In addition to th accelerator and suppressor species, levelers may also be added in the formulation to reduce or eliminate over-fill phenomenon discussed before in this application. Levelers get adsorbed preferentially on high-current density regions of the plated surface and help reduce this current density and thus protrusions th: would have resulted. A leveler concentration of 0.5-2mol/1 may be used for this purpose in addition to t accelerator and suppressor species in the exemplary high acid chemistry mentioned above. An exemplar leveler which is sold under the brand nameCubath) Via-Form Leveler is available from EnthonOMIt).

[00056] As illustrated in Figure 13B, once the no-touch plating with the first plating solution is complet an ECMD touch-plating stage using a second plating solution 136 forms a second layer 134b that coats first copper layer in anon-conformal fashion, depositing more materials into the cavities and less onto th surface regions where WSID sweeps. During this touch-plating process, as the second plating solution 1 is delivered onto the first copper layer 134a, WSID touches and mechanically sweeps the part of the firs layer 134a that is located on the field regions and over the small and mid size features. Combined with t chemistry of the second plating solution, the sweeping action of the WSID slows down the growth of th copper layer on the field region and above the small features which are already filled and accelerates growth of the copper layer in the large features, thus planarizes the overall Copper deposit. It should be noted that the touch-plating stage of the process may be terminated before total planarization is achievec the degree of planarization achieved at that point is adequate for simplifying the overburden removal process such as a CMP process, which follows the deposition process. In this embodiment, the additive chemistry of the second plating solution is optimized for the touch-plating step. For example, the seconc plating solution 132 may not contain any levelers. Furthermore, the accelerator-to-suppressor ratio in th second electrolyte may be higher than the ratio in the first electrolyte. Referring back to the exemplary high acid electrolyte mentioned above the accelerator concentration in the second electrolyte may be in range of 2-10ml/l, whereas the suppressor concentration may be in the 2-8ml/l. This can be done becaus all the small features have already been filled on the wafer by the first plating step and therefore there is danger of causing void formation in such features by these new additive concentrations, which if used during the first stage process would result in non-optimal filling of the small features. The second electrolyte may even contain a single additive which is an accelerator. The present inventors observed tl although single additive baths containing only suppressors or only accelerators could be used for planarization in an ECMD process, planarization was more efficient for the baths containing just accelerators compared to baths containing just suppressors.

[00057] Figure 14A shows the Focused Ion Beam (FIB) image of a 5-micron wide trench on a wafer wh was coated with copper using an ECMD apparatus and a copper sulfate electrolyte comprising Enthone Via-Form high acid VMS solution and8ml/1 of Cubath (D ViaForm Leveler. A charge of 4 A-min was passed between the 200 mm diameter substrate and a copper anode during this process and a WSID was contact with the wafer which was rotated at 50 rpm. As can be seen from the image in Figure 14A there relatively more copper deposited into the feature than onto the top surface of the substrate indicating pa planarization. Figure 14B shows the FIB cross-section taken from the same location of a similar wafer, which was processed similarly, however this time in another copper sulfate electrolyte comprising Enth Via-Form high acid VMS solution and 2.2ml/1 ofCubathX ViaFormT^ :
Accelerator. It is clear that copper deposition rate into the feature is higher in this case than the case in Figure 5a indicating better planarization efficiency. The copper film in the 5-micron trench of Figure 14 is completely planar. This example illustrates that the solution chemistry may be optimized for best planarization of a substrate during the touch-plating stage of the present invention.

[00058] The present invention allows optimization of the chemistry for the first stage of the process separate from the optimization of the chemistry for stage 2. This is important because although it is possible to use the same chemistry for both the first and second stage of the ECMPR as described in the above mentioned patents and patent applications, it is attractive and benefic to have the ability to optimize chemistry for the two stages independent from each other as will be furth described below.

[00059] Concentrations and types of additives used in the first stage of the subject process may vary depending upon the nature of the additives, nature of the small features, nature of the barrier/seed layers etc. For example, some accelerator species containing sulfur react with weak seed layers. If the seed lay is very thin on the side-walls of the vias for a specific wafer, it may be necessary to reduce the accelerat to-suppressor ratio in the electrolyte in the first stage of the process that is employed to coat this specific wafer. For other wafers with other types of seed layers it may be necessary to further adjust the relative concentrations of additives to obtain the best gap fill performance. If the over-fill over the dense array o small features presents a problem, it may be necessary to include leveler into the formulation in additior the accelerator and suppressors.

[00060] The electrolyte chemistry, which is adjusted for best gap fill in the first stage may not be the be for the second stage of the process when planarization takes place. For example, levelers are known to g attracted to high current density regions on the wafer surface.

However, ECMD process is known to accelerate growth in cavities on the substrate surface by increasin the deposition current density in such cavities compared to the top surface of the wafer swept by the WSID. Therefore, levelers in an electrolyte used for the second stage of the process may lower the planarization efficiency. This is an example of how presence of an additive (such as a leveler) in the process electrolyte may be favored during the first stage (no-touch step) of the process, whereas its presence may not be necessary or desired during the second stage (touch plating step). Similarly, a high accelerator-to-suppressor ratio may be desirable in the second stage than for the first stage of the proces described before. The experiment of Figure 14B indicated that an electrolyte containing only accelerato species may be successfully used in the second stage of the process, although such a formulation may n be successfully used for the first stage. Use of only one additive for the second process step may reduce total additive consumption, simplify additive measurement and control systems, reduce costs and impro planarization efficiency increasing throughput. Total impurity content of the deposited film may also be reduced by this approach.

[00061] In accordance with the principles of the present invention the first and the second stages of the process may be either performed in the same process module or multiple process modules. If the same process module approach is used to perform both stages, the first and second stages are performed sequentially, and using a first solution for the first stage and a second solution for the second stage. As fully described above, the first solution chemistry includes additives enhancing bottom up filling of the features on the wafer. And, the second solution chemistry includes only one or two of the three additive that may be used for the first stage and is optimized specifically to obtain a planar copper layer. If there multiple process modules, the first stage may be carried out in a first or first group of process modules v the first solution chemistry, and the second stage may be carried out with a second or second group of process modules using the second solution chemistry. Following the two-stage deposition, the wafer is cleaned and planar or near-planar copper overburden is removed using the CMP or other (e. g.,electropolishing) removal methods. The copper overburden may be removed before or after an anneal step.

[00062] It should be noted that after the second stage of the present process, optionally a third and even fourth step can be used to reduce the thickness of the copper overburden. After the second stage of the

process, the copper removal process may be performed as a third stage of the process that employs eithe an electrochemical etching or polishing stage or an ECME (electrochemical mechanical etching) stage. ' removal process may be also performed using both steps sequentially as a third and fourth stage, for example, a no-touch etching step that is followed by a touch ECME, or a touch ECME followed by a no touch etching. Thin planar deposits can be obtained by first depositing a planar layer using the ECMD technique at the first and second stages, and then electroetching this planar film in the same electrolyte (an electroetching solution by reversing the applied voltage. This way the thickness of the deposit may al be reduced in a planar manner. In fact, etching may be continued until all the metal on the field regions : removed. These techniques may be performed subsequent to second stage and using the second solution an electroetching solution while reversing the polarity of the applied voltage and rendering the workpie(surface more anodic compared to the electrode.

Alternatively, a third solution comprising an electroetching solution may replace the second solution at ı third stage and a fourth stage of the process, for example a no-touch electroetching (third stage) followe by a touch ECME (fourth stage). In this respect, a fourth stage such as a touch ECME process stage may performed using a fourth solution.

[00063] Figure 15 exemplifies a system 150 using multiple modules A, B, C and D. In this exemplary configuration, the modules A and B may be ECD or ECMD modules to perform the first stage of the process with a first process solution. The second stage of the process may be performed in module C, which may also be an ECMD module, using the second process solution.

Module D may be an ECME module to perform the above described third stage, such as a notouch stage electroetching or ECME using the second process solution or third process solution, or to perform a fou electroetching stage, such as a touch ECME, that uses the process solution that is used for the third stage a fourth process solution such as an electroetching solution.

Alternately the modules A, B, C and D may be ECD and ECMD modules carrying out the first and seco stages of the process using two different solutions as explained before. The number of each module will depend on the throughput of the first and the second stage processes. A robot would be used to transfer wafers between the various modules.

[00064] Figure 16 exemplifies a preferred system 200 using the single process module approach as appl to a two-step process. As shown in Figure 16, the system 200 comprising a first process module (PM1) : and a first process solution module (PSM1) 204. PM1 includes a process container 206 to hold process solutions and an electrode (anode) 208. The process container may have a volume less than two liters, preferably less than one liter. An upper opening 210 of the process container is enclosed with a WSID 2 Above the WSID 212, a wafer 214 to be processed by the process of the present invention is held by a wafer carrier 217.

ThePSM1 comprises a process solution supply unit 216, a first valve 218, a second valve 220 and a drai 222. The supply unit 216 supplies fresh process solutions to the process container via the first valve 218 The used solutions from the process container 206 is delivered back to the supply unit or to the drain 22 via the second valve 220.

[00065] Referring to Figure 16, the process supply unit 216 comprises a first tank 224 to store the first solution for the first stage of the process, a second tank 226 to store the second solution for the second stage of the process. Descriptions of the first solution, second solution, first stage and second stage are given in the above description. When the used solutions are received by the unit 216, their additive and plating solution chemistries are checked and then replenished so that the tanks 224,226 always keep process solutions with the right chemistries.

The supply unit 216 also includes a rinse tank228 to store DI water. DI water is used to clean the proces container 206 before the beginning of each process stage to. DI water may come directly from a DI line rather than from a tank. The tanks 224,226 and 228 are connected to the valve218 through supply lines 224', 226'and228'. The valve218 is connected to the process container206 through a line 230. Further, us solutions (first, second and the rinsing solutions) are brought to the valve 220 through the line 232. Fron the valve 220, the first solution is taken to first tank via line 234, the second solution is taken to second tank via line 236. The rinsing solution from the valve 220 is directed to the drain 222.

[00066] In an exemplary process sequence, at the first stage of the process, the first process solution fro the first solution tank224 of the PSM1 is delivered, via the valve 218, to the process solution container 2 of the PM1 and circulated back through return line 236. After the wafer 214 is processed the valve 218 i turned to DI supply and DI water from the rinse tank 228 is delivered to the process container 206 via th valve218 to clean the process container from the residues of the first solution. During the cleaning, the valve 218 may be periodically turned off and the valve 220 is turned on to direct the used rinsing solutic to the drain 222.

After the rinsing the second stage of the process is performed similar to the first stage but using the fresl second solution from the second tank 226 and delivering the used second solution back to second solutic tank 226 for the replenishment and storage purposes. After the second stage of the process, the process container is once again rinsed for the following wafer to be processed with the process of the present invention. It should be noted that there are many ways of feeding the various solutions to the process module. The example given here is just one of many possibilities. In case the two solutions used in this example are compatible, the rinse steps in between may be skipped and small amount of intermixing between the solutions may be allowed.

[00067] It should be understood, of course, that the foregoing relates to preferred embodiments of the invention and that modifications may be made without departing from the spirit and scope of the inventi

Claims of corresponding document: **WO03009361**

What is claimed is:

1. An electrochemical processing method for operating upon a wafer, the wafer having a top surface wit first and second cavities disposed thereon, the first cavity having a narrower width than a second cavity, and a conductive layer having a conductive top surface associated therewith disposed on the top surface the wafer and on the first and second cavities, the method comprising: performing electrochemical deposition on the conductive layer of the wafer using a first electrolyte solution having a first conductiv material therein to result in at least the first cavity being at least partially filled with the first conductive material ; and performing electrochemical mechanical deposition on the conductive layer of the wafer ir which the first cavity is at least partially filled with the first conductive material using a second electroly that has a second conductive material therein to result in at least some of any remaining cavity of the fir and second cavities being further filled with the second conductive material, wherein physical contact ar relative motion is maintained between the conductive top surface of the conductive layer disposed over top surface of the wafer and a workpiece surface influencing device for at least a period of the electrochemical mechanical deposition.

2. A method according to claim 1 wherein the first electrolyte solution is different from the second

electrolyte solution.

3. The method according to claim 2 wherein both the first electrolyte solution and the second electrolyte solution contain an accelerator additive and a suppressor additive.

4. The method according to claim 3 wherein acceleration activity within the second electrolyte solution higher than the acceleration activity within the first electrolyte solution.

5. The method according to claim 2 wherein the steps of performing electrochemical deposition and performing electrochemical mechanical deposition are performed in different process modules and each the first electrolyte solution and the second electrolyte solution are each delivered to a different one of tl different process modules.

6. The method according to claim 2 wherein the first electrolyte solution is optimized to fill the first cav without defects and wherein the second electrolyte solution is optimized for planar deposition.

7. The method according to claim 2 wherein the conductive layer is initially a seed layer and wherein th first electrolyte solution is selected based upon a characteristic of the seed layer.

8. The method according to claim 2 wherein the steps of performing electrochemical deposition and performing electrochemical mechanical deposition are performed in a same process module and each of the first electrolyte solution and the second electrolyte solution are delivered to the same process modul

9. The method according to claim 8 further including the step of cleansing the same process module witl cleaning solution between the steps of performing electrochemical deposition and performing electrochemical mechanical deposition.

10. The method according to claim 1 wherein the first electrolyte solution is the same as the second electrolyte solution 11. The method according to claim 1 wherein the steps of performing electrochemic deposition and performing electrochemical mechanical deposition are performed in a same process module.

12. The method according to claim11, wherein during at least a substantial period of the electrochemica deposition, deposition occurs without physical contact between the wafer and the workpiece surface influencing device 13. The method according to claim 12 wherein during the substantial period the electrochemical deposition occurs with the workpiece surface influencing device spaced a distance from the wafer, thereby allowing for the workpiece surface influencing device to operate as a shaping plate.

14. The method according to claim 11 wherein the step of performing electrochemical deposition occurs that during substantially an entire period thereof the electrochemical deposition occurs without physical contact between the wafer and the workpiece surface influencing device.

15. The method according to claim 14 wherein the period of the electrochemical mechanical deposition substantially an entire time that the step of performing electrochemical mechanical deposition is performed.

16. The method according to claim 1 wherein during substantially an entire period that the step of performing electrochemical mechanical deposition is performed the physical contact and the relative motion is maintained between the conductive top surface of the conductive layer disposed over the top surface of the wafer and the workpiece surface influencing device.

17. The method according to claim 16 wherein the step of performing electrochemical deposition occurs that during substantially an entire period thereof the electrochemical deposition occurs without physical contact between the wafer and any workpiece surface influencing device.

18. The method according to claim 1 wherein the step of performing electrochemical deposition minimi. the formation of a conductive bump over the first cavity by applying a reverse pulse potential. depositio occurs without physical contact between the wafer and any workpiece surface influencing device.

18. The method according to claim 1 wherein the step of performing electrochemical deposition minimi. the formation of a conductive bump over the first cavity by applying a reverse pulse potential.

19. The method according to claim 1 wherein the step of performing electrochemical mechanical deposition results in the conductive top surface of the conductive layer being planar and each of the first and second cavities being completely filled.

20. The method according to claim 1 wherein the step of performing electrochemical deposition is performed until a depth of the first cavity is less than the width of the first cavity.

21. The method according to claim 1 further including the step of performing electrochemical etching of the conductive layer after the step of performing electrochemical mechanical deposition.

22. The method according to claim 21 wherein during at least a period of the step of electrochemical etching the electrochemical etching occurs without physical contact between the wafer and a workpiece surface influencing device.

23. The method according to claim 21 wherein the step of performing electrochemical etching of the conductive layer uses electrochemical mechanical etching and during the step of performing electrochemical mechanical etching physical contact and relative motion is maintained between the conductive top surface of the conductive layer disposed over the top surface of the wafer and the workpiece surface influencing device for at least a period of the electrochemical mechanical etch.

24. The method according to claim 21 wherein the step of performing electrochemical etching uses an electrolyte solution that is also used during the steps of performing electrochemical deposition and performing electrochemical mechanical deposition.

25. The method according to claim 1 wherein, after the step of performing electrochemical mechanical deposition, repeating at least one of the steps of performing electrochemical deposition and performing electrochemical mechanical deposition until the any remaining cavity of the first and second cavities are completely filled with one of the first and second conductive materials.

26. The method according to claim 25 wherein the first and second conductive materials are the same.

30. The method according to claim 1 wherein the conductive material is copper.

31. An integrated circuit manufactured including the method of claim 1.